IN THE CLAIMS

Please cancel Claims 17, 18, and 24 without prejudice or disclaimer.

Claim 1 (currently amended): A digital amplifier including a noise shaper and a dither generator arranged to introduce noise to the shaper, said generator using a seed value derived from a ~~state-variable~~ delay element of said shaper.

Claim 2 (original): A digital amplifier as claimed in claim 1 and wherein the number of bits in the generated noise exceeds that of the seed value.

Claim 3 (original): A digital amplifier as claimed in Claim 1 or Claim 2 and wherein the dither generator includes shift registers of predetermined bit lengths to receive said seed values and provide a noise output.

Claim 4 (original): A digital amplifier as claimed in any preceding claim including means for scaling said noise.

Claim 5 (withdrawn): A digital amplifier including a clocked modulator wherein clock activity is monitored by counting divided multiples of the clock.

Claim 6 (withdrawn): A digital amplifier as claimed in claim 5 and including multiple clocks and wherein a first clock is used to count a second clock.

Claim 7 (withdrawn): A digital amplifier as claimed in claim 6 and wherein a divided multiple of said second clock is counted.

Claim 8 (withdrawn): A digital amplifier as claimed in any of claims 5 to 7 and wherein output is disabled when a clocking error is detected.

Claim 9 (withdrawn): A digital amplifier as claimed in any of claims 5 to 8 and wherein when a clocking error is detected, a parameter indicative of the error is stored.

Claim 10 (withdrawn): A digital amplifier having a detection arrangement to provide an error signal when there is no modulator drive or clock loss or undefined input states to an h-bridge leg.

Claim 11 (withdrawn): A digital amplifier having a deadtime generation or control arrangement substantially as herein described.

Claim 12 (withdrawn): A digital amplifier in which deadtime is balanced on rising and falling edges of signals.

Claim 13 (withdrawn): A digital amplifier in which deadtime is adaptive to gate charge of the output switching device.

Claim 14 (withdrawn): A digital amplifier in which deadtime is temperature independent or temperature compensated.

Claim 15 (withdrawn): A digital amplifier having programmable deadtime control or inter-channel delay or ABD delay which may be optimized by means of programming registers.

Claim 16 (withdrawn): A digital amplifier as claimed in claim 15 and wherein deadtime is controlled by a resistor or programming register.

Claims 17 and 18 (cancelled)

Claim 19 (withdrawn): A digital amplifier including means for reducing the effect of peak or spike voltages from the power supply.

Claim 20 (withdrawn): A digital amplifier as claimed in claim 19 and wherein said means comprises a clamp diode in association with power supply filtering.

Claim 21 (withdrawn): An integrated half bridge device laid out substantially as herein described.

Claim 22 (withdrawn): An integrated half bridge device with pin out substantially as herein described or equivalent thereto.

Claim 23 (withdrawn): A digital amplifier having high side over current protection substantially as herein described.

Claim 24 (cancelled)